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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/762,315	01/23/2004	Tsukio Funaki	XA-10024	4641

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MILES & STOCKBRIDGE PC
1751 PINNACLE DRIVE
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EXAMINER	
MATISIAK, JENNIFER E	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 02/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/762,315	FUNAKI, TSUKIO	
	Examiner	Art Unit	
	Jennifer Matisiak	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- if NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *7* is/are allowed.

6)☒ Claim(s) *1-6 and 8* is/are rejected.

7)☒ Claim(s) *9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 January 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02/06/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. Claims 2 and 8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 2, applicant does not disclose what is meant by "wherein a stress between the semiconductor chip and the substrate is relaxed by thinning the adhesive layer." Thinning the substrate may be interpreted as curing the adhesive layer, molding the adhesive layer or etching the surface layer of the adhesive. Additionally, applicant discloses the following "the stress between the bump electrode 5 connected with the mounting substrate and the interconnect 2 of the tape substrate 3 is relaxed by *thickening* the plated film 11" (p. 27); "according to the present invention, *thickening* of the pad formed the end portion the interconnect effective for relaxing the stress formed between the bump electrode connected to a mounting substrate and the interconnect of the tape substrate" (p. 36, para 7). Since the applicant does not disclose the manner in which the substrate is to be thinned and due to the pithy evidence in the disclosure regarding thickening the substrate to decrease stress on the device, the claim is rendered indefinite.

2. The term "sufficient thickness" in claim 8 is a relative term which renders the claim indefinite. The term "sufficient thickness" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

Claim Objections

3. Claim 3 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claim 3 is dependent on claim 2 which does not recite the limitation "wherein a solder resist covers the interconnect of the substrate", therefore claim 3 is does not further limit claim 2.

Drawings

4. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the common interconnect disposed along the periphery of the substrate and the number of the stud bumps to be connected to the common interconnect, as recited in claim 7, being greater than the number of the external terminals to be connected to the common interconnect

must both be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency.

Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

5. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Imasu et al. US 64927371, hereinafter Imasu. Imasu discloses a semiconductor device (1 of Fig. 4, for example) having a semiconductor chip (12) mounted over a substrate (4) in which an

interconnect (6a) is formed, by using an adhesive layer (20) to permit contact conduction between a stud bump (13a) of the semiconductor chip and an interconnect of a tape substrate (col 6, lines 45, 52), wherein over the stud bump (13a), another stud bump (13b) is stacked to form a multistage stud bump structure.

6. Claims 2-6 and 8 rejected under 35 U.S.C. 102(b) as being anticipated by Hosomi et al. (US 2001/0027007)

Regarding claim 2, Hosomi discloses a semiconductor device (1 of Fig. 1, for example) having a semiconductor chip (20) mounted over a substrate (10) in which an interconnect (14) is formed, by using an adhesive layer (50) to permit contact conduction between a stud bump (30) of the semiconductor chip and an interconnect of a tape substrate (para [0029]).

Hosomi does not explicitly disclose "wherein a stress between the semiconductor chip and the substrate is relaxed by thinning the adhesive layer." However:

"[E]ven though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985)

Therefore, no patentable weight is given to the product-by-process claim limitation because the device disclosed in the invention of Hosomi and the device of the instant invention are structurally equivalent.

Regarding claim 3, Hosomi discloses a semiconductor device wherein a solder resist covering the interconnect of the substrate is omitted (as shown in Fig. 1).

Regarding claim 4, Hosomi discloses a semiconductor device (1) having a semiconductor chip (20) mounted over a substrate (10) in which an interconnect (14) is formed, by using an adhesive layer (50) to permit contact conduction between a stud bump (30) of the semiconductor chip and an interconnect of a tape substrate (para [0029]), wherein an interconnect formation surface at the end portion of the substrate is covered with the adhesive layer (as shown in Fig. 1).

Regarding claim 5, Hosomi discloses a semiconductor device wherein the substrate is a flexible tape substrate (para [0029]).

Regarding claim 6, Hosomi discloses a semiconductor device wherein the adhesive layer is a thermosetting adhesive (para [0047]). Furthermore, it is well known in the art that encapsulant or protective resin is cured under heat becoming a rigid structure thereby constituting a thermosetting material.

Regarding claim 8, Hosomi discloses a semiconductor device (1 of Fig. 1) having a semiconductor chip (20) mounted over a substrate (11) in which an interconnect (14) is formed by using an adhesive layer (50) to connect a stud bump (30) of the

semiconductor chip to one end of the interconnect and an external terminal (15) of the semiconductor device to the other end of the interconnect, wherein a bump electrode (15) which will be an external terminal is formed, via a pad (13), at the other end of the interconnect and the pad is formed to have sufficient thickness.

Allowable Subject Matter

7. Claim 7 is allowed. The prior art on record does not teach alone or in combination, a device that uses "an adhesive layer to connect a stud bump of the semiconductor chip to one end of the interconnect and an external terminal of the semiconductor device to the other end of the interconnect."

8. Claim 9 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer Matisiak whose telephone number is 571-272-2639. The examiner can normally be reached on Business Days 9:30a-6:30p EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 517-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Douglas W. Owens

JEM

DOUGLAS W. OWENS
PRIMARY EXAMINER

2/15/06